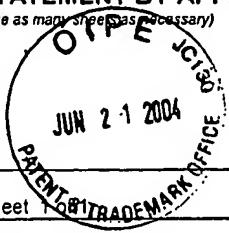


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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known				
 Sheet 1 of 1		Application Number	10/786,726			
		Filing Date	February 25, 2004			
		First Named Inventor	Forbes, Leonard			
		Group Art Unit	2818			
		Examiner Name	Unknown			
		Attorney Docket No: 303.680US3				

US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
M	US-6,297,103	10/02/2001	Ahn, Kie , et al.	438	275	02/28/2000
/	US-6,384,448	05/07/2002	Forbes, Leonard	257	315	02/28/2000
/	US-6,456,535	09/24/2002	Forbes, Leonard , et al.	365	185.28	06/15/2001
/	US-6,605,961	08/12/2003	Forbes, L.	326	41	02/29/2000
/	US-6,639,835	10/28/2003	Forbes, L.	365	186.14	02/29/2000
/	US-6,720,221	04/13/2004	Ahn, Kie , et al.	438	275	08/30/2001
M	US-6,730,960	05/04/2004	Forbes, L.	257	321	08/30/2001

EXAMINER

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Substitute Disclosure Statement Form (PTO-1449)

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1. Applicant's unique citation designation number (optional) 2. Applicant is to place a check mark here if English language Translation is attached

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	Unknown
		Filing Date	Even Date Herewith
		First Named Inventor	Forbes, Leonard
		Group Art Unit	Unknown
		Examiner Name	Unknown
Sheet 1 of 3		Attorney Docket No: 303.680US3	

US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
<i>Any</i>	US-3,387,286	06/04/1968	Dennard, Robert H.	340	173	07/14/1967
	US-4,051,354	09/27/1977	Choate, W. C.	235	312	07/03/1975
	US-4,313,106	01/26/1982	Hsu, Sheng T.	340	825.91	06/30/1980
	US-4,471,240	09/11/1984	Novosel, D.	307	463	08/19/1982
	US-5,105,388	04/14/1992	Itano, K. , et al.	365	189.08	12/26/1990
	US-5,327,380	07/05/1994	Kersh III, D. V. , et al.	365	195	02/08/1991
	US-5,406,524	04/11/1995	Kawamura, Shouichi , et al.	365	226	01/25/1994
	US-5,455,791	10/03/1995	Zaleski, Andrzej , et al.	365	185.26	06/01/1994
	US-5,464,785	11/07/1995	Hong, G.	437	43	11/30/1994
	US-5,555,206	09/10/1996	Uchida, T.	365	149	10/04/1995
	US-5,559,449	09/24/1996	Padoan, S. , et al.	326	40	02/21/1995
	US-5,579,259	11/26/1996	Samachisa, G. , et al.	365	185.14	05/31/1995
	US-5,608,670	03/04/1997	Akaogi, T. , et al.	365	185.23	05/08/1995
	US-5,646,428	07/08/1997	Hamada, Minoru	257	239	06/16/1995
	US-5,671,178	09/23/1997	Park, J. , et al.	365	185.22	02/05/1996
	US-5,706,227	01/06/1998	Chang, Shang-De T. , et al.	365	185.,18	12/07/1995
	US-5,740,104	04/14/1998	Forbes, Leonard	365	185.03	01/29/1997
	US-5,754,477	05/19/1998	Forbes, Leonard	365	185.33	01/29/1997
	US-5,790,455	08/04/1998	Caywood, John M.	365	185.96	01/02/1997
	US-5,801,401	09/01/1998	Forbes, Leonard	257	77	01/29/1997
	US-5,811,865	09/22/1998	Hodges, Robert L. , et al.	257	411	12/16/1996
	US-5,852,306	12/22/1998	Forbes, Leonard	257	315	01/29/1997
	US-5,936,274	08/10/1999	Forbes, Leonard , et al.	257	315	07/08/1997
	US-5,959,896	09/28/1999	Forbes, L.	365	185.33	02/27/1998
	US-5,973,356	10/26/1999	Noble, Wendell P. , et al.	257	319	07/08/1997
	US-5,991,225	11/23/1999	Forbes, Leonard , et al.	365	230.06	02/27/1998
	US-6,100,559	08/08/2000	Park,	257	315	08/14/1998
	US-6,124,729	09/26/2000	Noble, Wendell P. , et al.	326	41	02/27/1998
<i>Any</i>	US-6,137,725	10/24/2000	Caser, F. T. , et al.	365	185.23	12/02/1998
	US-6,222,224	04/24/2001	Shigyo, N.	257	315	12/19/1997
<i>Any</i>	US-6,246,089	06/12/2001	Lin, Yai-Fen , et al.	257	315	03/13/2000

EXAMINER

Ryan Hoang

DATE CONSIDERED

7/2004

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	Unknown
		Filing Date	Even Date Herewith
		First Named Inventor	Forbes, Leonard
		Group Art Unit	Unknown
		Examiner Name	Unknown
Sheet 2 of 3		Attorney Docket No: 303.680US3	

	US-6,249,460	06/19/2001	Forbes, Leonard , et al.	365	185.28	02/28/2000
	US-6,351,428	02/26/2002	Forbes, Leonard	365	230.06	02/29/2000

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	JP-60-046125	03/12/1985	Nakamura, H.	H03K	19/177	

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ²
hny		"Frequently-Asked Questions (FAQ) About Programmable Logic", http://www.OptiMagic.com/faq.html , (1997),15 pages				
		CHEN, J. , et al., "Hot Electron Gate Current and Degradation in P-Channel SOI MOSFET's", 1991 IEEE International SOI Conference Proceedings, Vail Valley, Colorado,(October 1991),pp.8-9				
		DIPERT, BRIAN , "Flash Memory Goes Mainstream", <u>IEEE Spectrum</u> , 30(10), (October 1993),48-52				
		FRANK, J. , et al., "Monte Carlo Simulations of p- and n-Channel Dual-Gate Si MOSFET's at the Limits of Scaling", <u>IEEE Transactions on Electron Devices</u> , 40(11), (November 1993),pg. 2103				
		GHODSI, RAMIN , et al., "Gate-Induced Drain-Leakage in Buried-Channel PMOS-A Limiting Factor in Development of Low-Cost, High-Performance 3.3-V, 0.25- μ m Technology", <u>IEEE Electron Device Letters</u> , 19(9), (September 1998),354-356				
		HODGES, D. A., et al., <u>Analysis and Design of Digital Integrated Circuits</u> , McGraw-Hill Book Company, 2nd Edition,(1988),394-396				
		MOORE, WILL R., "A Review of Fault-Tolerant Techniques for the Enhancement of Integrated Circuit Yield", <u>Proceedings of the IEEE</u> , 74(5), (May 1986),684-698				
		MULLER, D. A., "The Electronic Structure at the Atomic Scale of Ultrathin Gate Oxides", <u>Nature</u> , 399, (June 1999),758-761				
		OHGURO, T. , et al., "10th Micron P-MOSFET's with Ultra Thin Epitaxial Channel Layer Grown by Ultra-High Vacuum CVD", <u>IEDM</u> , Washington, D.C.,(1993),pp. 433-436				
		OHNAKADO, T. , et al., "1.5V Operation Sector-Erasable Flash Memory with Bipolar Transistor Selected (BITS) P-Channel Cells", <u>1998 Symposium on VLSI Technology; Digest of Technical Papers</u> , (1998),14-15				
hny		OHNAKADO, T. , et al., "Novel Electron Injection Method Using Band-to-Band Tunneling Induced Hot Electron (BBHE) for Flash Memory with a P-Channel Cell", <u>1995 International Electron Devices Meeting TECHNICAL DIGEST</u> , Washington D.C.,,(1995),pp. 279-282				

EXAMINER

hny

DATE CONSIDERED

7/2004

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <small>(Use as many sheets as necessary)</small>		<i>Complete if Known</i>
		Application Number Unknown Filing Date Even Date Herewith First Named Inventor Forbes, Leonard Group Art Unit Unknown Examiner Name Unknown
Sheet 3 of 3		Attorney Docket No: 303.680US3

<i>hj</i>	OHNAKADO, T. , et al., "Novel Self-Limiting Program Scheme Utilizing N-Channel Select Transistors in P-Channel DINOR Flash Memory", <u>1996 International Electron Devices Meeting TECHNICAL DIGEST</u> , San Francisco, CA,(1996),pp. 181-184	
	PAPADAS, C. , "Modeling of the Intrinsic Retention Characteristics of FLOTOX EEPROM Cells Under Elevated Temperature Conditions", <u>IEEE Transaction on Electron Devices</u> , 42, (April 1995),678-682	
	PATEL, N. K., et al., "Stress-Induced Leakage Current in Ultrathin SiO ₂ Films", <u>Appl. Phys. Letters</u> , 64(14), (April 1994),1809-1811	
	RHYNE, In: <u>Fundamentals of Digital Systems Design</u> , Prentice Hall, New Jersey,(1973),pg. 70-71	
	SALM, C. , et al., "Gate Current and Oxide Reliability in p+ Poly MOS Capacitors with Poly-Si and Poly-Ge0.3Si0.7 Gate Material", <u>IEEE Electron Device Letters</u> 19(7), (July 1998),213-215	
<i>✓</i>	SHI, YING, et al., "Tunneling Leakage Current in Ultrathin (<4 nm) Nitride/Oxide Stack Dielectrics", <u>IEEE Electron Device Letters</u> , 19(10), (October 1998),388-390	
<i>hm</i>	WU, Y. , et al., "Time Dependent Dielectric Wearout (TDDW) Technique for Reliability of Ultrathin Gate Oxides", <u>IEEE Electron Device Letters</u> , 20(6), (June 1999),262-264	

EXAMINER

Glenn Horwitz

DATE CONSIDERED

7/2004